VLSI-SoC 2013 Program

OCTOBER 6, 2013 SUNDAY

IFIP TC 10.5 Meeting (with invitation) **15:00-16:50**
Organizer: Dominique Borrione, IMAG, France
Room: Golden Horn

Coffee Break **16:50-17:10**

VLSI-SoC 2013 TPC Meeting (with invitation) **17:10-19:00**
Organizer: Alex Orailoğlu, UC San Diego, USA and Luigi Carro, UFRGS, Brazil
Room: Golden Horn

OCTOBER 7, 2013 MONDAY

Registration **8:00-8:30**

Opening **8:30-9:00**
General Chairs, Program Chairs, Local Officials
Room: Marmara I/II/III

Monday Keynote: "VLSI 2.0: R&D Post Moore" **9:00-10:00**
Sani Nassif, IBM Austin Research Lab, USA
Chair: H. Fatih Uğurdağ, Özyeğin University, Turkey
Room: Marmara I/II/III

Coffee Break **10:00-10:20**

M1A (Regular Session): Analog and Mixed-Signal IC Design 1 **10:20-12:00**
Chair: Salvador Mir, TIMA Laboratory, France
Room: Marmara I/II

1. *A 0.7-V 400-nW Fourth-Order Active-Passive ΔΣ Modulator with One Active Stage*
   Ali Fazli Yeknami and Atila Alvandpour
   Linköping University, Sweden
2. *A New Compact Analog VLSI Model for Spike Timing Dependent Plasticity*
   Mostafa Rahimi Azghadi, Said Al-Sarawi, Nicolangelo Iannella, and Derek Abbott
   The University of Adelaide, Australia

3. *Fully Electronically Programmable Complex Filter for Multi-standard Applications*
   Hussain Alzaher and Noman Tasadduq
   King Fahd University of Petroleum and Minerals, Saudi Arabia
4. *Single-Stage Amplifiers with Gain Enhancement and Improved Energy-Efficiency Employing Voltage-Combiners (short)*
   Ricardo Póvoa, Nuno Lourenço, Nuno Horta, Rui Santos-Tavares, and João Goes
   TU Lisbon and Universidade Nova de Lisboa (UNL), Portugal
5. *Design Considerations for Low Gain Amplifier in the MDAC of Digitally Calibrated Pipelined ADCs (short)*
   Hussein Adel, Marie-Minerve Louerat, and Marc Sabut
   Pierre & Marie Curie University and STMicroelectronics, France

M1B (Regular Session): Circuits and Systems for Applications 1 **10:20-12:00**

Chair: İlker Hamzaoğlu, Sabancı University, Turkey
Room: Marmara III

1. *A Real-Time 720p Feature Extraction Core Based on Semantic Kernels Binarized*
   Michael Schaffner, Pascal Hager, Lukas Cavigelli, Pierre Greisen, Frank Gürkaynak, and Hubert Kaeslin
   ETH and Disney Research, Switzerland
2. *On the Design of Modulo 2^n±1 Residue Generators*
   Kostas Tsoumanis, Constantinos Efstathiou, Nikos Moschopoulos, and Kiamal Pekmestzi
   National Technical University of Athens and Technological Institute of Athens, Greece
3. *An Area-Efficient Minimum-Time FFT Schedule using Single-Ported Memory*
   Stephen Richardson, Ofer Shacham, Dejan Markovic, and Mark Horowitz
   Stanford University, USA
4. *An Inverter-Based Neural Amplifier for Neural Spike Detection*
   Sungho Kim and Urs Frey
   RIKEN Quantitative Biology Center Kobe, Japan

M1C (Special Session 1): Emerging Research in the Region **10:20-12:00**

Chair: Özgür Sinanoğlu, NYU Abu Dhabi, United Arab Emirates
Room: Golden Horn

1. *Effects of the Positive Feedback Loop in Self Biased Bandgap Reference Circuits (ext. abstract)*
   Kemal Ozanoğlu and Selçuk Talay
   Dialog Semiconductor, Turkey
2. *Improved Hardware Security in ASIC Design Flow using Wire Scrambling Methodology (ext. abstract)*
   Sharareh Zamanzadeh and Ali Jahanian
   Shahid Beheshti University, Iran
3. *Graph Based Fault Model Definition for Bus Testing (ext. abstract)*
   Elmira Karimi, Mohammad Hashem Haghbayan, Adele Maleki, and Mahmoud Tabandeh

Sharif University of Technology, University of Tehran, and Science and Research Branch Islamic Azad University, Iran

4. *On the Accuracy of Monte Carlo Yield Estimators (ext. abstract)*
   Alp Arslan Bayrakçi
   Gebze Institute of Technology, Turkey
5. *High-Speed Binary Signed-Digit RNS Adder with Posibit and Negabit Encoding (ext. abstract)*
   Somayeh Timarchi, Maryam Saremi, Mahmood Fazlali, and Georgi Gaydadjiev
   Shahid Beheshti University, Iran
   Chalmers University of Technology, Sweden
6. *Implementation of Neuro-Fuzzy System based image edge detection (ext. abstract)*
   Manel Elloumi, Mohamed Krid, and Dorra Sellami Masmoudi
   University of Sfax and University of Gabès, Tunisia
7. *Step Response Analysis of Third Order Opamps With Slew-rate (ext. abstract)*
   Mohsen Hassanpourghadi and Mohammad Sharifkhani
   Sharif University of Technology, Iran
8. *Multi-Band Tunable Low Noise Amplifiers Operating at 850MHz and 1900MHz Standards (ext. abstract)*
   Farshad Eshghabadi, Fatemeh Banitorfian, Norlaili Mohd Noh, Mohd Tafir Mustaffa, Asrulnizam Abd Manaf, and Othman Sidek
   Universiti Sains, Malaysia
9. *A ΔΣ Modulator Automated Synthesis Tool for Wireless Standards (ext. abstract)*
   Houda Daoud, Samir Ben Selem, and Mourad Loulou
   University of Sfax, Tunisia

Lunch **12:00-13:30**

M2A (Embedded Tutorial 1): Cell-Aware Test – from Gates to Transistors **13:30-15:10**
Janusz Rajski, Director, Mentor Graphics, USA
Chair: Miodrag Potkonjak, UCLA, USA
Room: Marmara I/II

M2B (Regular Session): Prototyping, Verification, and Validation **13:30-15:10**
Chair: Miguel Silveira, INESC ID / IST - TU Lisbon, Portugal
Room: Marmara III

1. *Analog Layer Extensions for Analog/Mixed-Signal Assertion Languages*
   Doğan Ulus, Alper Şen, and Faik Başkaya
   Boğaziçi University, Turkey
2. *SyntHorus-2: Automatic Prototyping from PSL*
   Katell Morin-Allory, Fatemeh Javaheri, and Dominique Borrione
   TIMA Laboratory, France
3. *A Debugging Method for Gate Level Circuit Designs by Introducing Programmability*
   Kosuke Oshima, Takeshi Matsumoto, and Masahiro Fujita
   The University of Tokyo, Japan

4. *On the Development of Diagnostic Test Programs for VLIW Processors*
   Davide Sabena, Matteo Sonza Reorda, and Luca Sterpone
   Politecnico di Torino, Italy

M2C (Regular Session): VLSI Test and Diagnosis **13:30-15:10**

Chair: Lorena Anghel, TIMA Laboratory, France
Room: Golden Horn

1. *New Techniques for Selecting Test Frequencies for Linear Analog Circuits*
   Mohand Bentobache, Ahcène Bounceur, Reinhardt Euler, Yann Kieffer, and Salvador Mir
   University of Bejaia, Algeria
   University of Brest, University of Grenoble Alpes, and TIMA Laboratory, France
2. *Thermal-Aware Test Scheduling for NOC-Based 3D Integrated Circuits*
   Dong Xiang, Gang Liu, Krishnendu Chakrabarty, and Hideo Fujiwara
   Tsinghua University, China
   Duke University, USA
   Osaka Gakuin University, Japan
3. *Power-Aware SoC Test Optimization through Dynamic Voltage and Frequency Scaling*
   Vijay Sheshadri, Vishwani Agrawal, and Prathima Agrawal
   Auburn University, USA
4. *FOF: Functional Observable Fault and its ATPG Techniques (short)*
   Masahiro Fujita, Takeshi Matsumoto, and Satoshi Jo
   University of Tokyo, Japan

Coffee Break and Posters **15:10-15:50**

Which papers' posters: Short papers and ext. abstracts in M{1,2}{A,B,C}
Chair: H. Fatih Uğurdağ, Özyeğin University, Turkey
Poster locations: Ask the Chair

M3A (Regular Session): Embedded Systems and Logic/High Level Synthesis **15:50-17:30**

Chair: Andreas Gerstlauer, UT Austin, USA
Room: Marmara I/II

1. *Minimization of EP-SOPs via Boolean Relations*
   Anna Bernasconi, Valentina Ciriani, Gabriella Trucco, and Tiziano Villa
   Universita di Pisa, Universita degli Studi di Milano, and Universita degli Studi di Verona, Italy
2. *A Basic-block Power Annotation Approach for Fast and Accurate Embedded Software Power Estimation*
   Chien-Min Lee, Chi-Kang Chen, and Ren-Song Tsay
   Synopsys, Industrial Technology Research Institute, and National Tsing-Hua University, Taiwan
3. *A Framework for Compiler Level Statistical Analysis over Customized VLIW Architecture*
   Amir Hossein Ashouri, Vittorio Zaccaria, Sotirios Xydis, Gianluca Palermo, and Cristina Silvano
   Politecnico di Milano, Italy

4. *Data Re-allocation Enabled Cache Locking for Embedded Systems (short)*
   Keni Qiu, Mengying Zhao, Chenchen Fu, and Chun Jason Xue
   City University of Hong Kong, China
5. *GR-PA: A Cost Pre-Allocation Model For Global Routing (short)*
   Leandro Nunes, Ricardo Reis, and Tiago Reimann
   Universidade Federal do Rio Grande do Sul, Brazil

M3B (Regular Session): Transistor Level Digital VLSI Circuits and Memory **15:50-17:30**

Chair: Roberto Murphy, Director de Formación Académica, INAOE
Room: Marmara III

1. *Gate Sizing in the Presence of Switching Activity and Input Vector Control*
   Nathaniel Conos, Saro Meguerdichian, and Miodrag Potkonjak
   University of California Los Angeles, USA
2. *An Accurate Power Estimation Model for Low-Power Hierarchical-Architecture SRAMs*
   Yuan Ren and Tobias Noll
   RWTH Aachen University, Germany
3. *Characterization of Mode Transition Timing Overhead for Net Energy Savings in Low-Noise MTCMOS Circuits*
   Hailong Jiao and Volkan Kurşun
   The Hong Kong University of Science and Technology, China
4. *Performance-driven SRAM Macro Design with Parameterized Cell Considering Layout-dependent Effects*
   Yu Zhang, Gong Chen, Qing Dong, Mingyu Li, and Shigetoshi Nakatake
   The University of Kitakyushu, Japan

M3C (Regular Session): Nanoscale Logic Fabrics – the Status of Switches **15:50-17:30**

Chair: Ian O'Connor, Ecole Centrale de Lyon, France
Room: Golden Horn

1. *Gate-controlled doping in carbon-based FETs*
   Joachim Knoch, Marcel Rene Mueller, and Thomas Grap
   Aachen University and TU Dortmund University, Germany
2. *Fine grain Multi-VT co-integration methodology in UTBB-FDSOI*
   A. Valentian, E. Beigne, P. Flatresse, B. Pelloux-Prayer, F. Clermidy
   CEA LETI and STMicroelectronics, France
3. *Spin-electronics Based Logic Fabrics*
   Weisheng Zhao
   IEF, France
4. *Reconfigurable Photonic Switching: towards All-Optical FPGAs*
   S. Le Beux, Z. Li, I. O'Connor
   INL, France

Future of Chip Design in Turkey (with invitation) and How It can Benefit from Fatih Project **17:45-19:15**

Organizers: Faruk Dönmez, Vestel-Vestek and H. Fatih Uğurdağ, Özyeğin University, Turkey
Room: Marmara I/II

International Microelectronics Olympiad of Armenia – Qualifier Round (with invitation) **18:00-20:00**

Organizer: H. Fatih Uğurdağ, Özyeğin University, Turkey
Room: Marmara III

IFIP TC 10 Meeting (with invitation) **17:30-19:15**

Organizer: Ricardo Reis, UFRGS, Brazil
Room: Golden Horn

Cocktail Party (at Zeyrekhane, shuttles will be available) **19:15-22:15**

OCTOBER 8, 2013 TUESDAY

Tuesday Keynote: "The Run-time System: Part of the OS or part of the chip design?" **9:00-10:00**

Yale Patt, The University of Texas at Austin, USA
Chair: Alex Orailoğlu, UC San Diego, USA
Room: Marmara I/II/III

Coffee Break **10:00-10:20**

T1A (Embedded Tutorial 2): Better-than-Worst-Case Timing Designs **10:20-12:00**

Adit Singh, Professor, Auburn University, USA and Abhijit Chatterjee, Professor, Georgia Tech, USA
Chair: Zain Navabi , University of Tehran, Iran
Room: Marmara I/II

T1B (Regular Session): Reconfigurable/Adaptive Systems and FPGA **10:20-12:00**

Chair: Smail Niar, LAMIH, Univ. of Valenciennes, France
Room: Marmara III

1. *Architecture and Implementation of Real-Time 3D Stereo Vision on a Xilinx FPGA*
   Sotiris Thomas, Kyprianos Papadimitriou, and Apostolos Dollas
   Technical University of Crete, Greece
2. *Three-Dimensional Stacking FPGA Architecture Using Face-to-Face Integration*
   Tetsuro Hamada, Qian Zhao, Motoki Amagasaki, Masahiro Iida, Morihiro Kuga, and Toshinori Sueyoshi
   Kumamoto University, Japan
3. *Implementation of Core Coalition on FPGAs*
   Kaushik Mysur, Mihai Pricopi, Thomas Marconi, and Tulika Mitra
   National University of Singapore, Singapore
4. *Low Cost FPGA Design and Implementation of a Stereo Matching System for 3D-TV Applications*
   Aydın Aysu, Murat Sayınta, and Cevahir Çığla

Virginia Tech, USA
Vestek and Aselsan, Turkey

T1C (Regular Session): Energy Minimization **10:20-12:00**

Chair: Chengmo Yang, University of Delaware, USA
Room: Golden Horn

1. *Dynamic Cache Pooling for Improving Energy Efficiency in 3D Stacked Multicore Processors*
   Jie Meng, Tiansheng Zhang, and Ayşe Coşkun
   Boston University, USA
2. *Energy Impact in the Design Space Exploration of Loop Buffer Schemes in Embedded Systems*
   Antonio Artes, Robert Fasthuber, Jose L. Ayala, Praveen Raghavan, and Francky Catthoor
   Complutense University of Madrid, Spain
   IMEC, Belgium
3. *Adapting the Columns of Storage Components for Lower Static Energy Dissipation*
   Mehmet Burak Aykenar, Muhammet Özgür, Osman Seçkin Şimşek, and Oğuz Ergin
   TOBB University of Economics and Technology, Turkey
4. *Static Energy Minimization of 3D Stacked L2 Cache with Selective Cache Compression*
   Jongbum Park, Jongpil Jung, Kang Yi, and Chong-Min Kyung
   KAIST and Handong Global University, Korea

Lunch **12:00-13:30**

T2A (Regular Session): Variability, Security, and Reliability **13:30-15:10**

Chair: Wenjing Rao, University of Illinois at Chicago, USA
Room: Marmara I/II

1. *New Scan-Based Attack Using Only the Test Mode*
   Sk Subidh Ali, Samah Mohamed Saeed, Özgür Sinanoğlu, and Ramesh Karri
   NYU Abu Dhabi, UAE
   Polytechnic Institute of NYU, USA
2. *Examining Thread Vulnerability Analysis Using Fault-Injection*
   Işıl Öz, Haluk Rahmi Topçuoğlu, Mahmut Kandemir, and Oğuz Tosun
   Boğaziçi University and Marmara University, Turkey
   Pennstate University, USA
3. *A Direct Measurement Scheme of Amalgamated Aging Effects with Novel On-Chip Sensor*
   Nicoleta Cucu Laurenciu, Yao Wang, and Sorin D. Cotofana
   Delft University of Technology, Netherlands
4. *IP–Core Protection for a non-volatile Self-Reconfiguring SoC Environment (short)*
   Wael Adi, Shaza Zeitouni, Huang Xinchao, Marc Fyrbiak, Christian Kison, M. Jeske, and Z. Nahas
   Technische Universitat Braunschweig, Germany
5. *Online Periodic Test Mechanism for Homogeneous Many-core Processors (short)*
   Arezoo Kamran and Zain Navabi
   University of Tehran, Iran

T2B (Regular Session): Circuits and Systems for Applications 2 **13:30-15:10**

Chair: Luc Claesen, University Hasselt, Belgium

Room: Marmara III

1. *Generating Fast Logic Circuits for m-select n-port Round Robin Arbitration*
   H. Fatih Uğurdağ, Fatih Temizkan, and Sezer Gören
   Özyeğin University, Ericam Vision & Defence Tech., and Yeditepe University, Turkey
2. *Fine Grain Word Length Optimization for Dynamic Precision Scaling in DSP Systems*
   Seogoo Lee and Andreas Gerstlauer
   University of Texas at Austin, USA
3. *Compressed Look-Up Table based Real-Time Rectification Hardware*
   Abdulkadir Akın, İpek Baz, Luis Manuel Gaemperle, Alexandre Schmid, and Yusuf Leblebici
   EPFL, Switzerland
4. *An Energy Efficient Time-sharing Pyramid Pipeline for Multi-resolution Computer Vision (short)*
   Qiuling Zhu, Navjot Garg, Yun-Ta Tsai, and Kari Pulli
   Carnegie Mellon University and NVIDIA Research, USA
5. *A High Performance and Low Energy Hardware for Intra Prediction with Template Matching (short)*
   Yusuf Adıbelli and İlker Hamzaoğlu
   Sabancı University, Turkey

T2C: PhD Forum **13:30-15:10**

Chair: Mahmut Kandemir, Penn State University, USA

Room: Golden Horn

1. *Evaluation and Exploration of On-Chip Communication Schemes in MPSoCs (ext. abstract)*
   Poona Bahrebar
   Ghent University, Belgium
2. *Transistor Sizing for MOSFET and FINFET Devices (ext. abstract)*
   Gracieli Posser
   UFRGS, Brazil
3. *Integer Linear Programming for Design Space Exploration in Heterogeneous MPSoC (ext. abstract)*
   Dammak Bouthaina (will be presented by Smail Niar)
   University of Valenciennes, France
4. *Routing Environment of Inter-FPGA Signals Based on Iterative Approach*
   Mariem Turki
   LIP6 – UPMC, France
5. *Systematically and Quantitatively Optimized Area and Energy Efficient Matrix Decomposition Accelerators (ext. abstract)*
   Upasna Vishnoi
   RWTH Aachen University, Germany

6. *Design and Development of Nano-electronic Circuits and Architectures (ext. abstract)*
   Ioannis Vourkas
   Democritus University of Thrace (DUTh), Greece
7. *Design of Efficient Arithmetic Circuits for Realization of Floating Point Adder/Subtractor Units (ext. abstract)*
   Sreehari Veeramachaneni
   Birla Institute of Technology and Science – Pilani, India
8. *Design of Low Power Fused MAC Unit in High-Performance DSP Systems (ext. abstract)*
   Syed Ershad Ahmed
   Birla Institute of Technology and Science – Pilani, India
9. *Power Integrity Analysis and Discrete Optimization of Decoupling Capacitors (ext. abstract)*
   Jai Narayan Tripathi
   IIT Bombay, India
10. *Design Methodology and Development of Mixed Signal ASICs for Space Applications in Standard CMOS Technology (ext. abstract)*
    S. Sordo-Ibáñez
    Universidad de Sevilla, Spain
11. *Thread Vulnerability for Multicore Architectures (ext. abstract)*
    Işıl Öz
    Boğaziçi University, Turkey
12. *Resource Management Design in 3D Stacked Multicore Systems for Improving Energy Efficiency (ext. abstract)*
    Tiansheng Zhang
    Boston University, USA

Coffee Break and Posters *(of Tuesday's short papers and PhD Forum)* **15:10-15:50**

Which papers' posters: Short papers and ext. abstracts in M3{A,B,C} and all of Tuesday
Chair: H. Fatih Uğurdağ, Özyeğin University, Turkey
Poster locations: Ask the Chair

Bosphorus Cruise and Dinner (in Ortaköy, shuttles will be available) **17:00-23:00**

OCTOBER 9, 2013 WEDNESDAY

Wednesday Keynote: "Data Mining Trends in VLSI Test" **9:00-10:00**

Magdy Abadir, Freescale, USA
Chair: Luigi Carro, UFRGS, Brazil
Room: Marmara I/II/III

Coffee Break **10:00-10:20**

W1A (Special Session 2): Are processors the NAND gates of the future? 10:20-12:00

Chair: Barış Özgül, Xilinx, Ireland

Room: Marmara I/II

1. *Processors as SoC Building Blocks (ext. abstract)*
   Yankın Tanurhan and Pieter van der Wolf
   Synopsys, USA and Netherlands
2. *Software-Programmable Digital Pre-Distortion on the Zynq SoC (ext. abstract)*
   Barış Özgül, Jan Langer, Juanjo Noguera, and Kees Vissers
   Xilinx, Ireland
3. *Heterogeneous Tasking on SMP/FPGA SoCs: the Case of OmpSs and the Zynq (ext. abstract)*
   Antonio Filgueras, Eduard Gil, Carlos Alvarez, Daniel Jimenez, Xavier Martorell, Jan Langer, and Juanjo Noguera
   Barcelona Supercomputing Center and Universitat Politecnica de Catalunya, Spain
   Xilinx Research Lab, Ireland
4. *Automatic Mapping of OpenCV Based Systems on New Heterogeneous SoCs (ext. abstract)*
   Francisco-Jose Sanchis-Cases, Antonio Martinez-Alvarez, and Sergio Cuenca-Asensi
   University of Alicante, Spain
5. *Accelerating Software Radio: Iris on the Zynq SoC (ext. abstract)*
   Jonathan van de Belt, Paul D. Sutton, and Linda E. Doyle
   University of Dublin, Ireland

W1B (Regular Session): SOC Design and Interconnect 10:20-12:00

Chair: Manfred Glesner, Technical University Darmstadt, Germany

Room: Marmara III

1. *Staggered Latch Bus: A Reliable Offset Switched Architecture for Long On-Chip Interconnect*
   Melvin Eze, Ozcan Ozturk, and Vijaykrishnan Narayanan
   Pennsylvania State University, USA
   Bilkent University, Turkey
2. *Architectural exploration of a fine-grained 3D cache for high performance in a manycore context*
   Eric Guthmuller, Ivan Miro-Panades, and Alain Greiner
   CEA LETI and University of Pierre et Marie Curie, France
3. *A Power-Efficient Hierarchical Network-on-Chip Topology for Stacked 3D ICs*
   Debora Matos, Cezar Reinbrecht, Tiago Motta and Altamiro Susin
   UFRGS Institute of Informatics, Brazil
4. *PFT- A Low Overhead Predictability Enhancement Technique for Non-Preemptive NoCs (short)*
   Bharath Sudev and Leandro Soares Indrusiak
   The University of York, UK
5. *FPGA vs DSP: A Throughput and Power Efficiency Comparison for Hierarchical Enumerative Coding (short)*
   Yuhui Bai, Syed Zahid Ahmed, Imen Mhedhbi, Khalil Hachicha, Cédric Champion, Patrick Garda

and Bertrand Granado
Université Cergy Pontoise, Université Pierre et Marie Curie, and Université Paris Diderot, France

W1C (Regular Session): Emerging Devices, Circuits and Systems **10:20-12:00**

Chair: Volkan Kurşun, The Hong Kong University of Science and Technology, China
Room: Golden Horn

1. *PVT Variation Detection and Compensation Methods for High-Speed Systems*
   Vazgen Melikyan, Abraham Balabanyan, Armen Durgaryan, Harutyun Stepanyan, Karen Sloyan, Hovik Musayelyan, and Gayane Markosyan
   Synopsys, Armenia
2. *Towards the Least Complex Time-Multiplexed Constant Multiplication (short)*
   Levent Aksoy, Paulo Flores, and Jose Monteiro
   INESC-ID/IST TU Lisbon, Portugal
3. *Analysis of Ring Oscillator Structures to Develop a Design Methodology for RO-PUF Circuits (short)*
   Giray Kömürcü, Günhan Dündar, and Ali Emre Pusane
   TÜBİTAK and Boğaziçi University, Turkey
4. *Improved Read Voltage Margins with Alternative Topologies for Memristor-based Crossbar Memories (short)*
   Ioannis Vourkas, Dimitrios Stathis, and Georgios Ch. Sirakoulis
   Democritus University of Thrace, Greece
5. *Self-Adaptability for Fair Resource Distribution in Future Nanoelectronic Systems: Modeling and Protocols (short)*
   Soumya Banerjee, Kai Da Zhao, Wenjing Rao, and Milos Zefran
   University of Illinois at Chicago, USA
6. *A Framework to Accelerate Sequential Programs on Homogeneous Multicores (short)*
   Christopher Fletcher, Rachael Harding, Omer Khan, and Srinivas Devadas
   MIT and University of Connecticut, USA
7. *Blind-LMS Based Digital Background Calibration for a 14-Bit 200-MS/s Pipelined ADC (short)*
   Yajuan He and Qiang Li
   University of Electronic Science and Technology of China, China
   Aarhus University, Denmark

Lunch **12:00-13:30**

W2A (Embedded Tutorial 3): Breaking the Dynamic Power Barrier using Distributed-LC Resonant Clocking **13:30-15:10**

Matthew Guthaus, Professor, University of California Santa Cruz, USA
Chair: Sezer Gören, Yeditepe University, Turkey
Room: Marmara I/II

W2B (Regular Session): Analog and Mixed-Signal IC Design 2 **13:30-15:10**

Chair: Günhan Dündar, Boğaziçi University, Turkey
Room: Marmara III

1. *A 90-dB DC Gain High-Speed Nested Gain-Boosted Folded-Cascode Opamp*
   Yajuan He and Qiang Li
   University of Electronic Science and Technology of China, China
   Aarhus University, Denmark
2. *Power Dissipation Limits of CBSC-Based Pipelined Analog-to-Digital Converters*
   Majid Zamani, Clemens Eder, and Andreas Demosthenous
   University College London, UK
3. *Variation-Aware and Adaptive-Latency Accesses for Reliable Low Voltage Caches*
   Po-Hao Wang, Wei-Chung Cheng, Yung-Hui Yu, Tang-Chieh Kao, Chi-Lun Tsai, Pei-Yao Chang, Tay-Jyi Lin, Jinn-Shyan Wang, and Tien-Fu Chen
   National Chiao Tung University and National Chung Cheng University, Taiwan
4. *7.72 ppm/°C, Ultralow Power, High PSRR CMOS Bandgap Reference Voltage (short)*
   Hamouda Assia, Arnold Ruediger, and Bouguechal Nour-Eddine
   Technische Universität Berlin, Germany
   University of Batna, Algeria

W2C (Regular Session): Transistor Level Digital VLSI Circuits and Silicon Debug 13:30-15:10
Chair: Farshad Moradi, Aarhus University, Denmark
Room: Golden Horn

1. *Tagged Probabilistic Simulation Based Error Probability Estimation for Better-Than-Worst Case Circuit Design*
   Amr Tosson, Siddharth Garg, and Mohab Anis
   Mentor Graphics Corporation, Egypt
   University of Waterloo, Canada
2. *Automatic Addition of Reset in Asynchronous Sequential Control Circuits*
   Vikas Vij and Kenneth Stevens
   University of Utah, USA
3. *A 65-nm CMOS Area Optimized De-synchronization Flow for sub-VT Designs*
   Christoph Müller, Steffen Malkowsky, Oskar Andersson, Babak Mohammadi, Jens Sparsø, and Joachim Neves Rodrigues
   Lund University, Sweden
   Technical University of Denmark, Denmark
4. *A Center-Aligned Digital Pulse-Width Modulator for Envelope Modulation of Polar Transmitters (short)*
   Chien-Hung Kuo and Cin-De Jhang
   National Taiwan Normal University, Taiwan

Coffee Break and Posters *(of Wednesday's short papers and Special Session 2)* **15:10-15:50**

Which papers' posters: Short papers and ext. abstracts on Wednesday
Chair: H. Fatih Uğurdağ, Özyeğin University, Turkey
Poster locations: Ask the Chair

Panel: Regional/Global Collab. Models to Boost Chip Design Sector in the Middle East **15:50-17:30**

Organizer: Yervant Zorian, Chief Architect, Synopsys, USA
Moderator: Yankın Tanurhan, VP, Synopsys, USA
Room: Marmara I/II/III

Arda Bafra, Maxim Integrated – Istanbul, Turkey
Görkem Canverdi, Ericsson Microelectronics Design Center – Istanbul, Turkey
Andre Ivanov, UBC, Canada
Nazım Kadrizade, Dialog Semiconductor – Istanbul, Turkey
Baker Mohammad, Khalifa University, UAE
Zain Navabi, University of Tehran, Iran
Paolo Prinetto, Polito Torino, Italy
Michel Renovell, LIRMM, France
Yervant Zorian, on behalf of Synopsys-Armenia

Concluding Remarks (incl. the ones about next year's conf. in Mexico) **17:30-18:00**

General Chairs, Program Chairs, next year's Chair